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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,340	03/17/2004	Thomas Nulsen	NPT-65.0402	5585

7590 06/05/2007

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
06/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/803,340	NULSEN ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03-23-07*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,10-14 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-14* is/are allowed.

6)☒ Claim(s) *1-5 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *attached drawing*.

DETAILED ACTION

This is responsive to the amendment filed on 11-16-06. Applicant's arguments with respect to reference Yamamoto (US. 5,444,744) have been carefully considered but they are not deemed to be persuasive to overcome the reference. Thus, the claims remain rejected under Yamamoto. The rejection changes slightly for clarification.

Claim Objections

Claim 19 is objected to because of the following informalities: the recitation "said delayed clock signal" on lines 4-5 lacks antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-5 and 18-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and /or clarification is required.

Regarding claim 1, the recitation "an input signal" on lines 7-8 is indefinite because it is not clear as to this "an input signal" is the same or different than the "an input signal" in line 4. The recitation " said pass/fail indicator" on line 11 lacks antecedent basis. It is also not clear as to this " said pass/fail indicator" is the same or different than the " a pass/fail indicator signal" on line 7. The same rationale is applied to the recitation " said pass/fail indicator" in claim 5.

Regarding claims 18 and 19, the recitation "a monitored voltage" in indefinite because it is not clear what it is. This "a monitored voltage" can be signal (Vi) or signal (Vr) in figure 2A of the present application. Clarification is required.

Claims 2-4 and 20 are indefinite because of the technical deficiencies of claims 1 and 18.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4, 5 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamamoto et al. (USP. 5,444,744). See attached drawing.

Regarding claim 1, figure 8 of Yamamoto shows a clock based voltage deviation detector comprising:

a pulse module (X) having a pulse input for receiving a clock signal (CLK) and a pulse output (B) for outputting a stream of reset pulses;

an indicator module (Y) having a first indicator input (1) for receiving an input signal (I4), a second indicator input (2) for receiving a reference voltage (9b), a third indicator input (3) communicatively coupled to said pulse output (B) of said pulse module and an indicator output (L) for outputting a pass/fail indicator signal as a function of said stream of reset pulses (B) and a difference (A) between an input signal (I4) and a reference voltage (9b), and

a correlation module (Z) having a first correlation input (P) for receiving said clock signal (CLK), a second correlation input (M) communicatively coupled to said indicator output (L) of said indicator module (Y), wherein "an event of said pass/fail indicator is correlated to a period of said clock signal (CLK) at which said event occurred". Note that clock (CLK) is a controlling input signal to the correlation module (Z) thus; an event of said "pass/fail indicator" (correlation module Z) is correlated to a period of said clock signal (CLK) at which said event occurred.

Regarding claim 4, the indicator module comprises:

a comparator (9a) having a first comparator input for receiving said input signal (I4), a second comparator input for receiving said reference voltage (9b) and a comparator output for outputting a trip signal (A) as a function of a difference between said input signal and said reference voltage; and

a latch (11) having a first input communicatively coupled to said comparator output of said comparator, a second input communicatively coupled to said pulse output (B) and a latch output (M) for outputting "said pass/fail indicator" as a function of said trip signal (A) and said stream of reset pulses.

Regarding claim 5 figure 8 of Yamamoto shows the indicator module (Y) comprising a latch-enabled comparator (9a) having a first comparator input (1) for receiving said input signal (I4), a second comparator input (2) for receiving said reference voltage (9b), a third comparator input (3) communicatively coupled to said pulse output (B) of said pulse module and a comparator output for outputting "said pass/fail indicator" as a function of said stream of reset pulses and a difference (A) between said input signal and said reference voltage.

Regarding claim 18, figure 8 shows a clock based voltage deviation detector comprising:

a means (X) for generating a reset pulse stream (B) as a function of a clock signal (CLK);

a means (Y) for generating a pass/fail indicator signal (at node M) as a function of said reset pulse stream (B) and an event of a monitored voltage (I4); and

a means (Z) for correlating an event of said pass/fail indicator signal with a specific period of said clock signal (CLK) at which said event occurred.

Allowable Subject Matter

Claims 10-14 are allowed because the prior art (US. 5,444,744) fails to teach or suggest a clock based voltage deviation detector comprising a counter and a storage module.

Claims 2, 3, 19 and 20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. Claims 2, 3, 19 and 20 would be allowable because the prior a fails to teach or suggest a pulse module comprising a delay cell and an exclusive-OR gate as called for in claim 2; a correlation module comprising a counter and a storage module; clock based voltage deviation detector comprising a means for

generating a reset pulse stream and a means for further generating the pass/fail indicator signal as called for in claim 19.

Response to Arguments

In the Remarks, the Applicant argues that "Yamamoto does not support the Office's assertion". In fact, figure 8 of Yamamoto fully shows the claimed circuit. Figures 10A-10I show the signals at different points of the circuit of figure 8.

Figure 8 clearly shows clock based voltage deviation detector comprising a pulse module (circuit X) receiving clock (CLK) and outputting a stream of reset pulses at node (B); an indicator module (Y) receiving an input signal (I4), a reference voltage (9b) and an pulse output signal stream of reset pulses of the pulse module (X). The indicator module (Y) outputs at the output node (M) a pass/fail indicator signal as a function of the stream of reset pulses (B) and the difference (A) between an input signal (I4) and the reference voltage (9b). The correlation module is circuit (Z) having a first correlation input (P) for receiving clock signal (CLK), a second correlation input (N) coupled to the indicator output (M). The event of the pass/fail indicator signal is correlated to a specific period of the clock signal (CLK) at input node (P).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

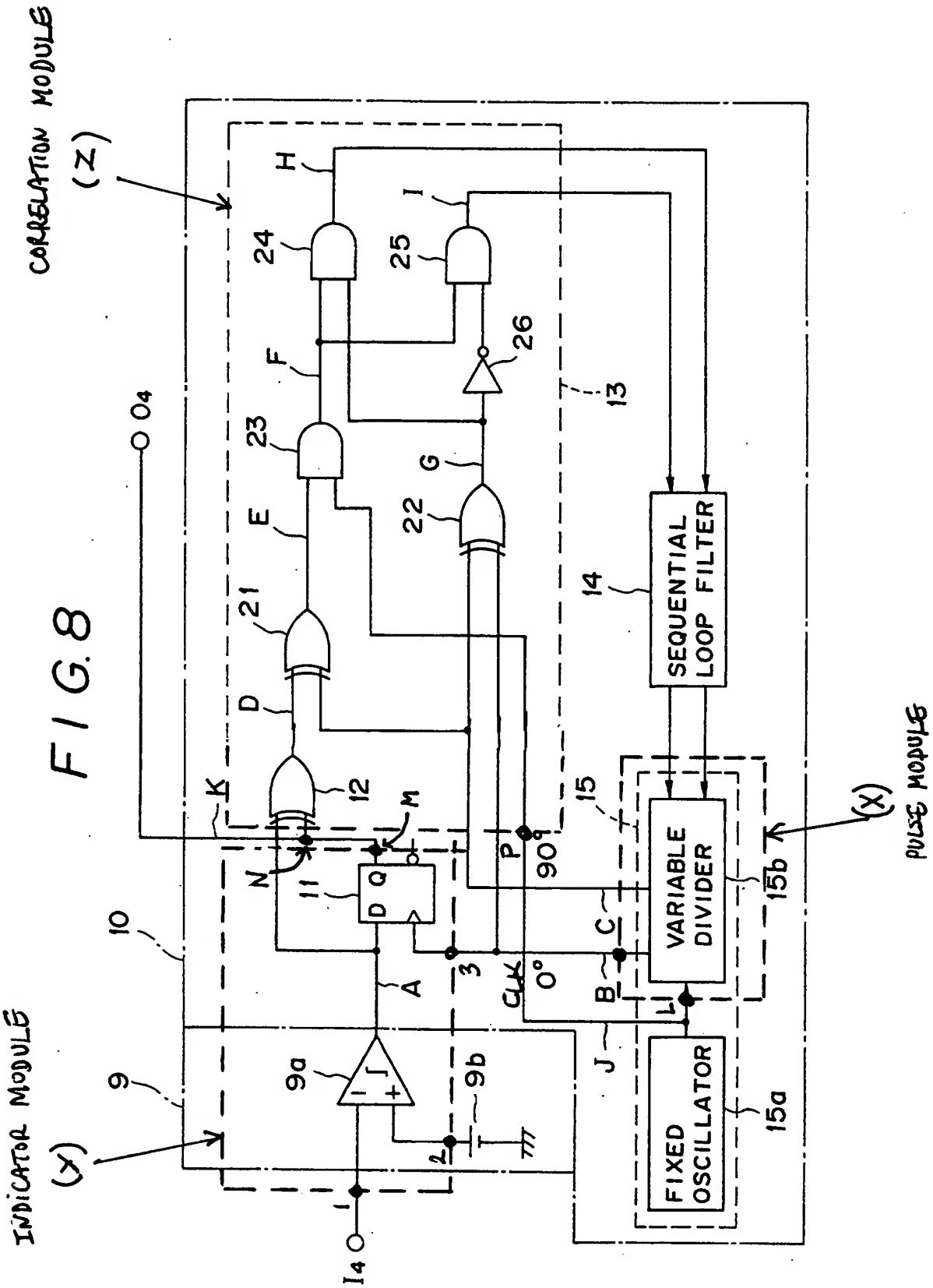
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hiep Nguyen

05-31-07

TUAN T. LAM
PRIMARY EXAMINER


CORRELATION MODULE
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INDICATOR MODULE
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PULSE MODULE
(X)
SEQUENTIAL LOOP FILTER
VARIABLE DIVIDER
FIXED OSCILLATOR
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FIG. 8